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10/715,015	11/17/2003	Jang-Won Moon	5649-1098	3312

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,015	MOON ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,15 and 16* is/are rejected.

7)☒ Claim(s) *11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

1. Claims 1-16 are pending in the application.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it exceeds 150 words in length.

Correction is required. See MPEP § 608.01(b).

3. Claims 11, 13 and 15 are objected to because of the following informalities:

Claim 11 recites a "NOR" circuit and a "NOR" operation which appears to be referring to 230 in Fig. 2; however, 230 is conventionally known in the art as a "NAND" circuit. It will be understood as such.

Claim 13 recites "the latching/inverting circuit" which appears to lack an antecedent basis. It will be understood as being dependent on claim 11.

Claim 15 recites "one of a first precharge control signal" which appears to be in error. The phrase "one of" should be deleted.

Claim 15 recites "logically OR'ing the column bank address and the second delayed signal to generate a second signal" which appears to lack proper antecedent basis in the figures or in the specification.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (U.S. Pat. No. 5,828,612) in view of Admitted Prior Art ("Admission").

Yu, for example in Figs. 2-4, discloses a memory device, comprising: a data line (inherent); and a variable delay precharge circuit (Fig. 2) that receives an initiating signal (CLK 104) and a write enable signal (R/W 102) and that precharges the data line responsive to the initiating signal (see Fig. 4) at a time that is determined by a state of the write enable signal (the falling edge of the READ or the WRITE pulse of /PRECHARGE 110 in Fig. 3);

wherein the variable delay precharge circuit comprises: a precharge circuit operative to precharge the data line responsive to a precharge control signal (/PRECHARGE 110); a variable delay precharge control signal generator circuit that receives the initiating signal and the write enable signal and that delays the precharge control signal with respect to the initiating signal

responsive to the write enable signal (see the READ and the WRITE pulses of /PRECHARGE 110 in Fig. 3);

wherein the variable delay precharge control signal generator circuit comprises: a precharge control signal generator circuit that receives the initiating signal, that generates first and second delayed signals (DEFAULT PRECHARGE TRIGGER 216 and WRITE PRECHARGE TRIGGER 212, respectively), from the initiating signal, that are delayed by respective different first and second predetermined time periods (t2 and trailing t5, respectively, in Fig. 3) with respect to the initiating signal, and that applies to the precharge circuit, responsive to a precharge delay control signal (WRITE PRECHARGE ENABLE 210), a selected one (via 306) of a first precharge control signal (/READ PRECHARGE 220) generated from the first delayed signal and a second precharge signal (/WRITE PRECHARGE 218) generated from the second delayed signal; and a precharge delay control circuit (including 200) that generates the precharge delay control signal responsive to the write enable signal;

wherein the variable delay precharge circuit precharges the data line after the first predetermined time period following assertion of the initiating signal when the write enable signal indicates a read operation (see the READ pulse of /PRECHARGE 110 in Fig. 3), and wherein the variable delay precharge circuit precharges the data line after the second predetermined time period following assertion of the address signal when the write enable signal indicates a write operation (see the WRITE pulse of /PRECHARGE 110 in Fig. 3); wherein the second time period is shorter than the first time period (see /PRECHARGE 110 in Fig. 3 which shows the WRITE pulse being shorter than the READ pulse);

wherein the first precharge control signal rises in synchronization with a rising edge of the initiating signal and falls the first period of time after an immediately succeeding falling edge of the initiating signal (see the READ pulses of CLK 104 and /PRECHARGE 110 in Fig. 3), and wherein the second precharge control signal rises in synchronization with a rising edge of the column bank address signal and falls the second period of time after an immediately succeeding falling edge of the column bank address signal (see the WRITE pulses of CLK 104 and /PRECHARGE 110 in Fig. 3);

wherein the precharge delay control circuit causes application of the first precharge control signal after a read operation of the memory device (the READ pulse of /PRECHARGE 110 in Fig. 3) and application of the second precharge control signal after a write operation of the memory device (the WRITE pulse of /PRECHARGE 110 in Fig. 3).

However, Yu does not disclose that the initiating signal is a column bank address signal, and that the precharge circuit precharges a pair of data input/output lines.

Admission, in Figs. 1A and 1B, discloses a column bank address signal (CBA) from which a delayed signal (output of 10) is generated for a precharge control signal (PIOPRB), and a precharge circuit (including a PMOS transistor; see page 1, line 12) precharging a pair of data input/output lines (see page 1, line 14) responsive to the precharge control signal (PIOPRB).

Since memories with multiple banks that generate a column bank address signal to initiate a read/write operation and with a pair of data input/output lines that are precharged were common and well known in the art (as exemplified by Admission), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the Yu's

precharging means to such memories, for the purpose of increasing the frequency of operation in such memories (see for example Yu, column 2, lines 36-41).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (U.S. Pat. No. 5,828,612) in view of Admitted Prior Art ("Admission") as applied to claim 6 above, and further in view of Nitta et al. (U.S. Pat. No. 5,831,924).

The above Yu/Admission combination discloses a memory device as recited in claim 6, with the exception of the pair of data input/output lines being a pair of global input/output lines. Nitta discloses a pair of global input/output lines that are precharged (see for example column 3, lines 37-42). Since memories having a pair of global input/output lines that are precharged were common and well known in the art (as exemplified by Nitta), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the precharging means of the Yu/Admission combination to such memories, for the purpose of increasing the frequency of operation in such memories (see for example Yu, column 2, lines 36-41).

7. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art ("Admission") in view of Yu et al. (U.S. Pat. No. 5,828,612).

Admission, in Figs. 1A and 1B, discloses a method of generating a precharge control signal for a precharge circuit of a memory device, the method comprising: receiving a column bank address signal (CBA); generating first delayed signal (the output of 10) from the column bank address signal that are delayed by a first time period (that of 10); logically OR'ing (via 15) the column bank address signal and the first delayed signal to generate a first signal (the output

of 15); generating a first precharge control signal (PIOPRB) responsive to the first signal and a first state of a write enable signal (either the read state or the write state; see page 2, lines 17-19); wherein the first precharge control signal is generated responsive to a read operation of the memory device (since PIOPRB is generated after either a read or a write operation; see page 2, lines 17-19).

However, Admission does not disclose generating a second delayed signal from the column bank address signal that is delayed by a second time period; logically OR'ing the column bank address signal and the second delayed signal to generate a second signal; generating a second precharge control signal responsive to the second signal and a second state of the write enable signal; wherein the first time period is greater than the second time period; wherein the second the second precharge control signal is generated responsive to a write operation.

Yu, for example in Fig. 3, discloses that a second precharge control signal (the WRITE pulse of /PRECHARGE 110) is generated after a write operation, delayed by a second time period (t5) that is shorter than a first time period (t2) associated with a first precharge control signal (the READ pulse of /PREACHARGE 110) generated after a read operation.

Therefore, in view of Yu, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to generate a second precharge control signal after a write operation, using a method similar to that of Fig. 1A of Admission but with a shorter delay than that of Fig. 1A, such that the method includes generating a second delayed signal from the column bank address signal that is delayed by a second time period shorter than the first time period, logically OR'ing the column bank address signal and the second delayed signal to generate a second signal, and generating the second precharge control signal responsive to the

second signal and a second state (i.e., the write state) of the write enable signal, for the purpose of increasing the frequency of operation (see for example Yu, column 2, lines 36-41).

Allowable Subject Matter

8. Claims 11-14 (insofar as claim 13 is understood to depend on claim 11) are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 11, the prior arts of record do not disclose or suggest a precharge control circuit as recite in claim 11, and particularly, a latching/inverting circuit that receives, latches, and inverts the signal output from the NOR circuit and the first delay signal, and responsively outputs a signal.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hoekstra et al. (U.S. Pat. No. 4,802,129) discloses a dual precharge circuit.

Suh et al. (U.S. Pat. No. 5,349,560) discloses a second precharge circuit for a write operation.

Houston (U.S. Pat. No. 5,404,327) discloses different precharge control signals for read/write operations.

Jang et al. (U.S. Pat. No. 6,356,494) discloses different delays for read/write operations.

Dietrich et al. (U.S. Pat. No. 6,359,832) discloses different circuits with different delays for read/write operations.

Kumar et al. (U.S. Pat. No. 6,631,093) discloses a second precharge circuit for a write operation.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

12/6/05

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